UNIVERSITY OF MACAU
FACULTY OF SCIENCE AND TECHNOLOGY

SEMINAR

PHYSICAL DESIGN AUTOMATION OF A TRANSISTOR NETWORK

Date and Time: 29th May 2009 (Friday), 4:00 PM
Venue: Analog and Mixed-Signal VLSI Lab, Silver Jubilee Building, JLG 211-212, University of Macau

Prof. Ricardo Reis
Full Professor,
Federal University of Rio Grande do Sul, Porto Alegre, Brazil

Abstract: The talk will present a new approach for the physical design automation of integrated circuits where the layout can be seen as a network of transistors. The logic cells are designed on the fly, without the limitations that exists when using a cell library (number of functions, number of transistors, transistor sizing, area and power consumption). A cell generator allows the automatic design of cells composed by any transistor network (using simple gates or static CMOS complex gates - SCCG) and any transistor sizing. When the size of the transistor should be bigger than the cell height, the tool is able to do transistor folding. As the designer is free from the limitations of a cell library, it is possible to do a deep logic minimization where all needed logic cells will be generated on the fly. This allows a reduction on the number of needed transistors to implement a circuit. As consequence, the static power consumption will also be reduced. The cell generator provides cells with a compacted layout, allowing a significant transistor density. It is presented physical design automation strategies related to transistor topologies, management of routing in all layers, VCC and Ground distribution, clock distribution, contacts and vias management, body ties management, transistor sizing and folding and the how these strategies can improve the layout optimization. Some results are compared with the ones obtained with traditional standard cells tools (vendor's tools), showing the gain in area, delay and power consumption. The flexibility of the approach can also let the designers to define the layout parameters to cope with problems like tolerance to transient effects, yield improvement, printability, etc. The designer can also manage the sizing of transistors to reduce power consumption, without compromising the clock frequency.

Biography: Ricardo Reis is a full professor of the Federal University of Rio Grande do Sul, at Porto Alegre, Brazil, since1981. He studied Electrical Engineering at UFRGS- Federal University of Rio Grande do Sul at Porto Alegre, Brazil (1978). He got his Ph.D. degree from the Institut National Polytechnique de Grenoble, France (1983). Ricardo Reis is research level 1 of the CNPq (Brazilian National Science Foundation) and head of several research projects supported by Government Agencies and Industry. Past head of the Graduate Program in Computer Science at UFRGS, where is a thesis advisor. He is head of the Microelectronics Graduate Program at UFRGS.
Since January 2008 Ricardo is the vice-president of IEEE Circuits and Systems representing Region 9 (Latin America). He has published more than three hundred papers in journals and conferences proceedings. He is also author and co-author of several books. Ricardo Reis is a senior member of IEEE. He served as a General Chair or Program Chair of several conferences.
His research interests are Physical Design, Physical Design Automation, Design Methodologies, Digital Design, CAD, Circuits Tolerant to Radiation and Microelectronics Education.

The lectures are open to the public

For enquiry:
Analog and Mixed-Signal VLSI Lab
Tel. (853) 83978796
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